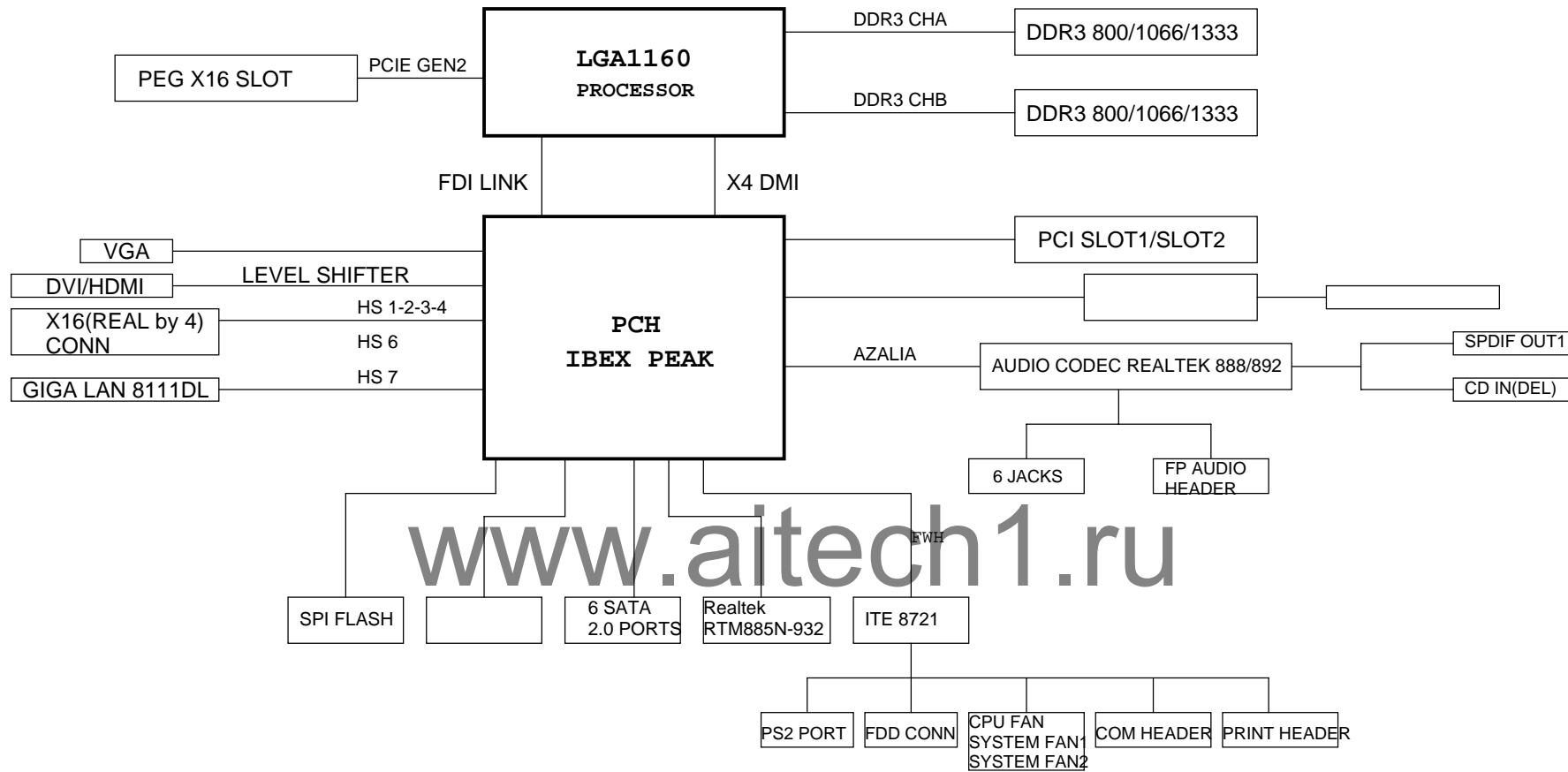
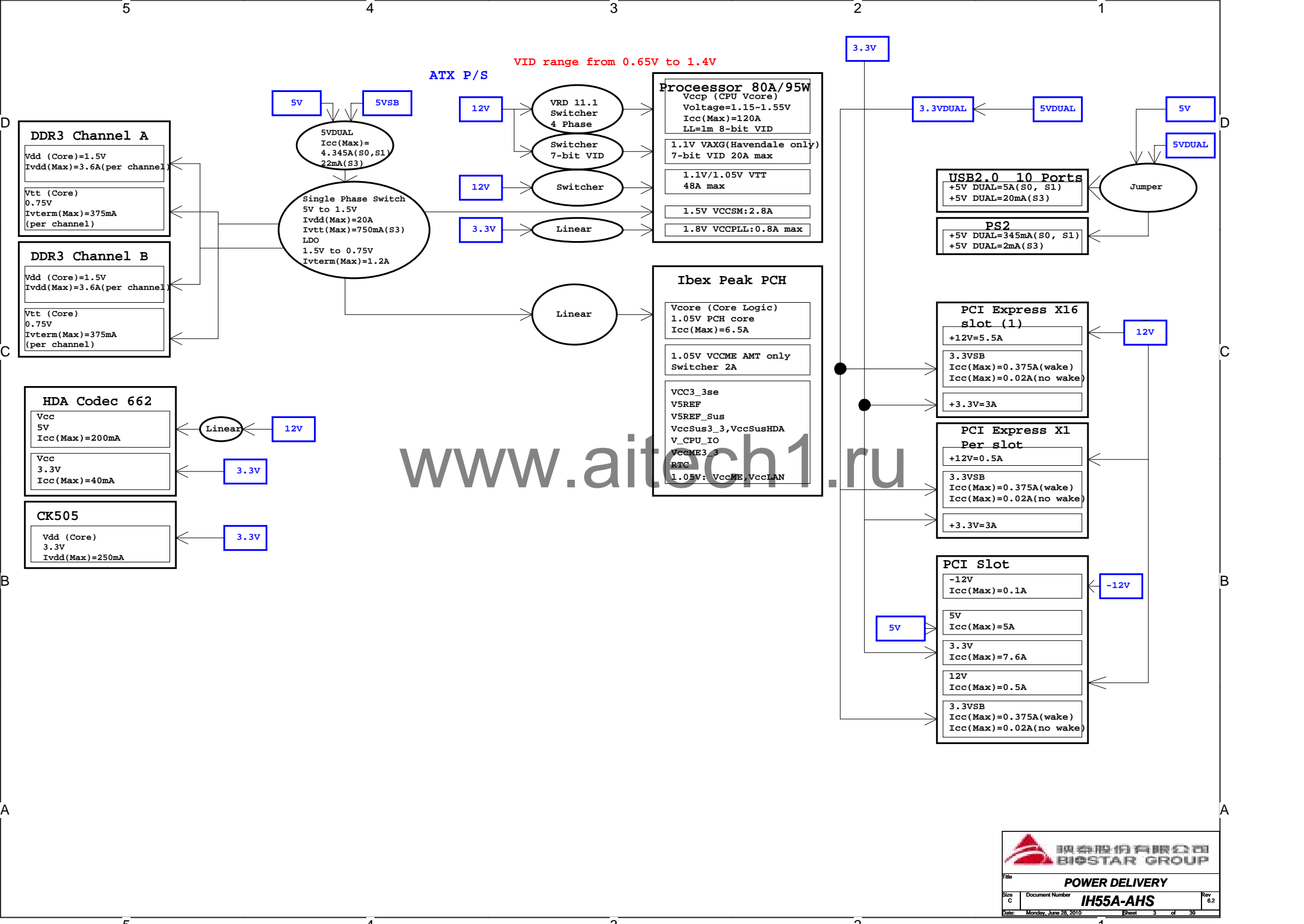


5 4 3 2 1



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5 4 3 2 1



Change From IH55E-MHT ver:6.1

- 1.uATX拉長為ATX
- 2.縮板寬for 24.9CM to 22.5 cm
- 3.增加一PCI-E X16 slot
- 4.增加MEMORY SLOT防盜鎖片
- 5.DEL IDE controllor-JMB363
- 6.DVI/HDMI共用一個level shift,用T型lay法
- 7.CLOCKGEN換成32 PIN RTM885-932
- 8.Del DEBUG LED

ver:0.6 to 6.0


- 1.修改防盜鎖片LAYOUT
- 2.SB改散熱片與IH55A-MHS共用SB散熱片

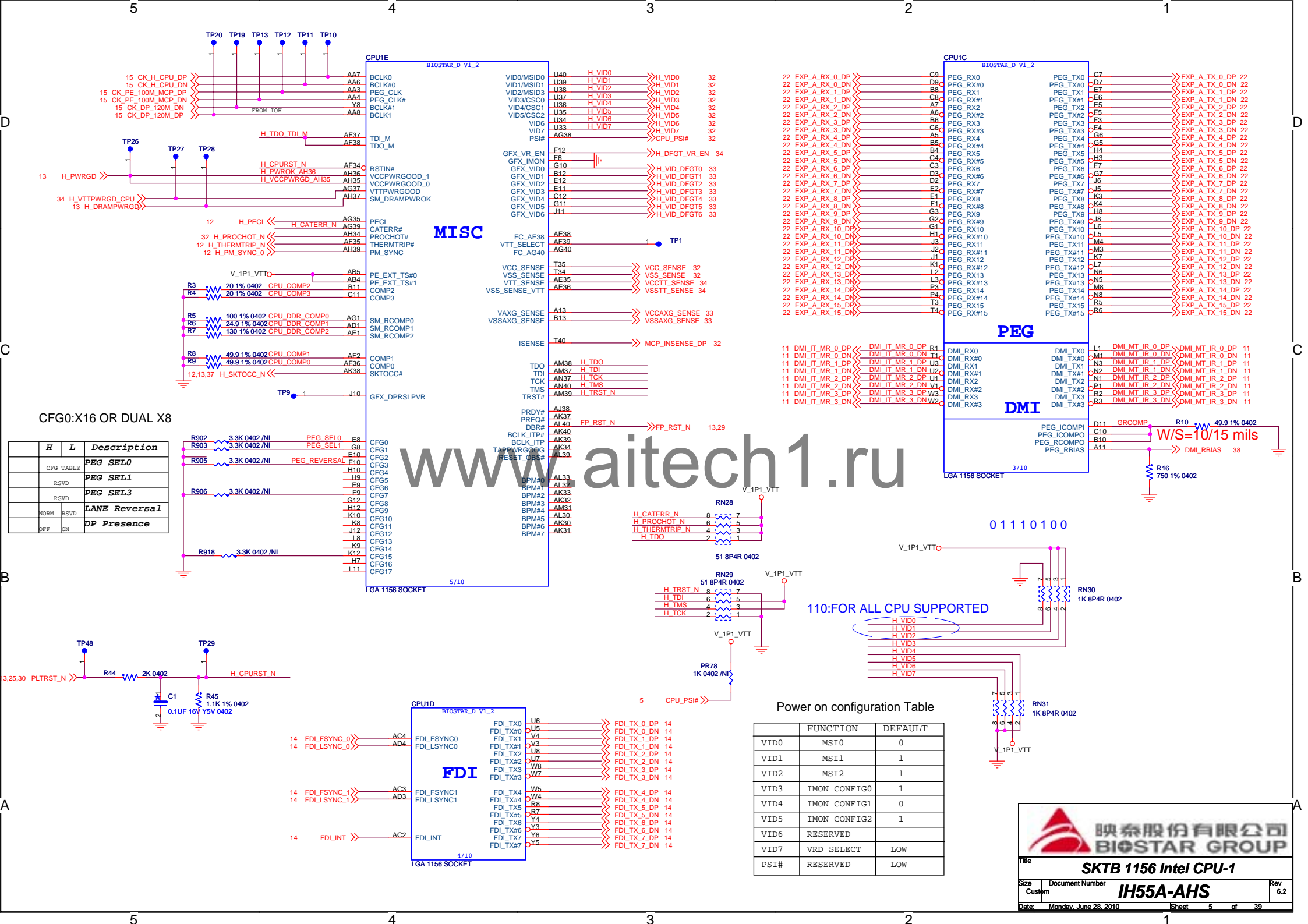
ver:6.0 to 6.1

- 1.Add VTTPWRGD decoupling CAP.(For sometime CPU-CORE POWER=0V when boot in OS.)
- 2.Add SIO H/W monitor VIN decoupling CAP.(solution do not have 12V,5V H/W monitor issse)
- 3.Correct colay CAP with OSC-CON and EC
- 4.Move output voltage CAP.CT42 from 1P05_ME to +3V3_DUAL
- 5.CT10 and CT45 colay with POWER_JUSB1
- 6.Reserved SPI ROM with SMT type
- 7.Add audio Front and Real Lineout CAP
- 8.Resvered PCH CLKREQ#0,2 and PEGCLK_B_RQ# pull down registor
- 9.Remove text with "EuP Ready"
- 10.Swap PCH A/B Chanel PEG CLOCK
- 11.Change GBE CLOCK from LANE 2 TO LANE 1
- 12.Change Broad ID for H/W mornitor 12V/5V ADJ

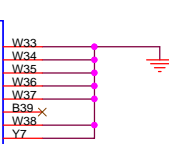
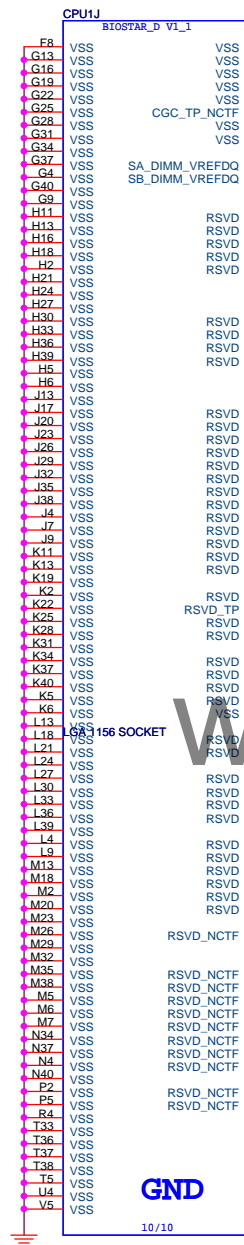
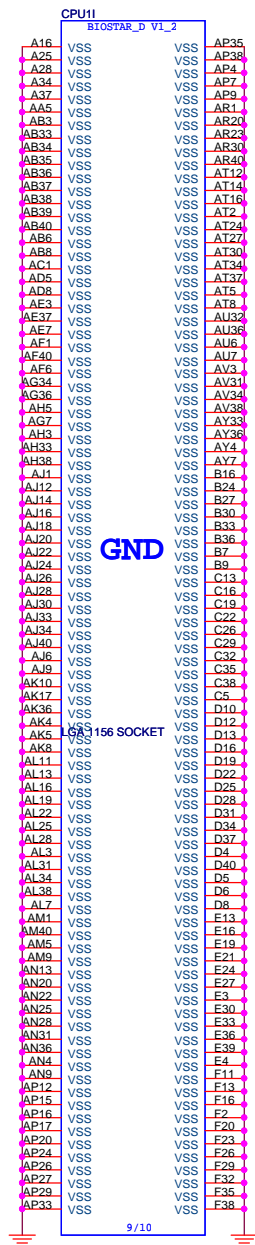
ver:6.1 to 6.2

解決工廠反映105P colay 0603與0402拋料不良過多問題,不再colay 0603,直接layout改0402

 映泰股份有限公司 BIOSAR GROUP			
Title REVISION HISTORY			
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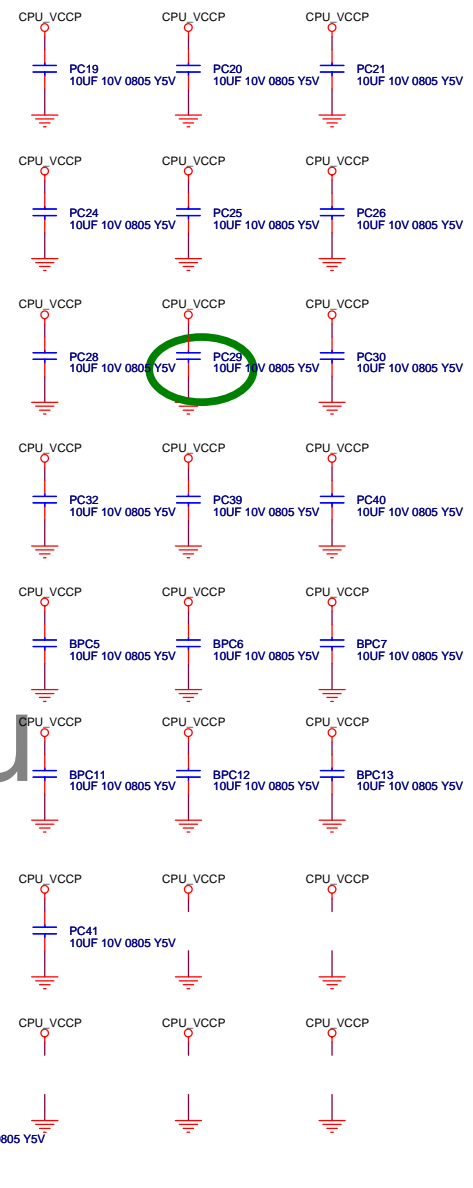
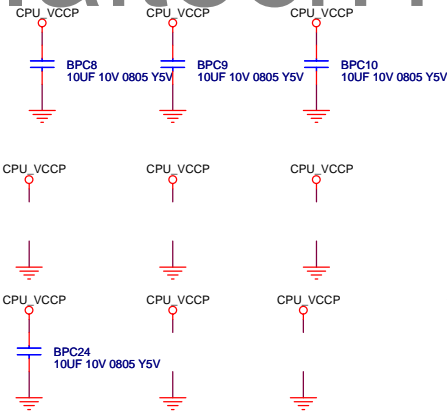


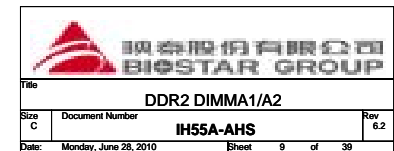
If reserved, only support Q3 version CPU

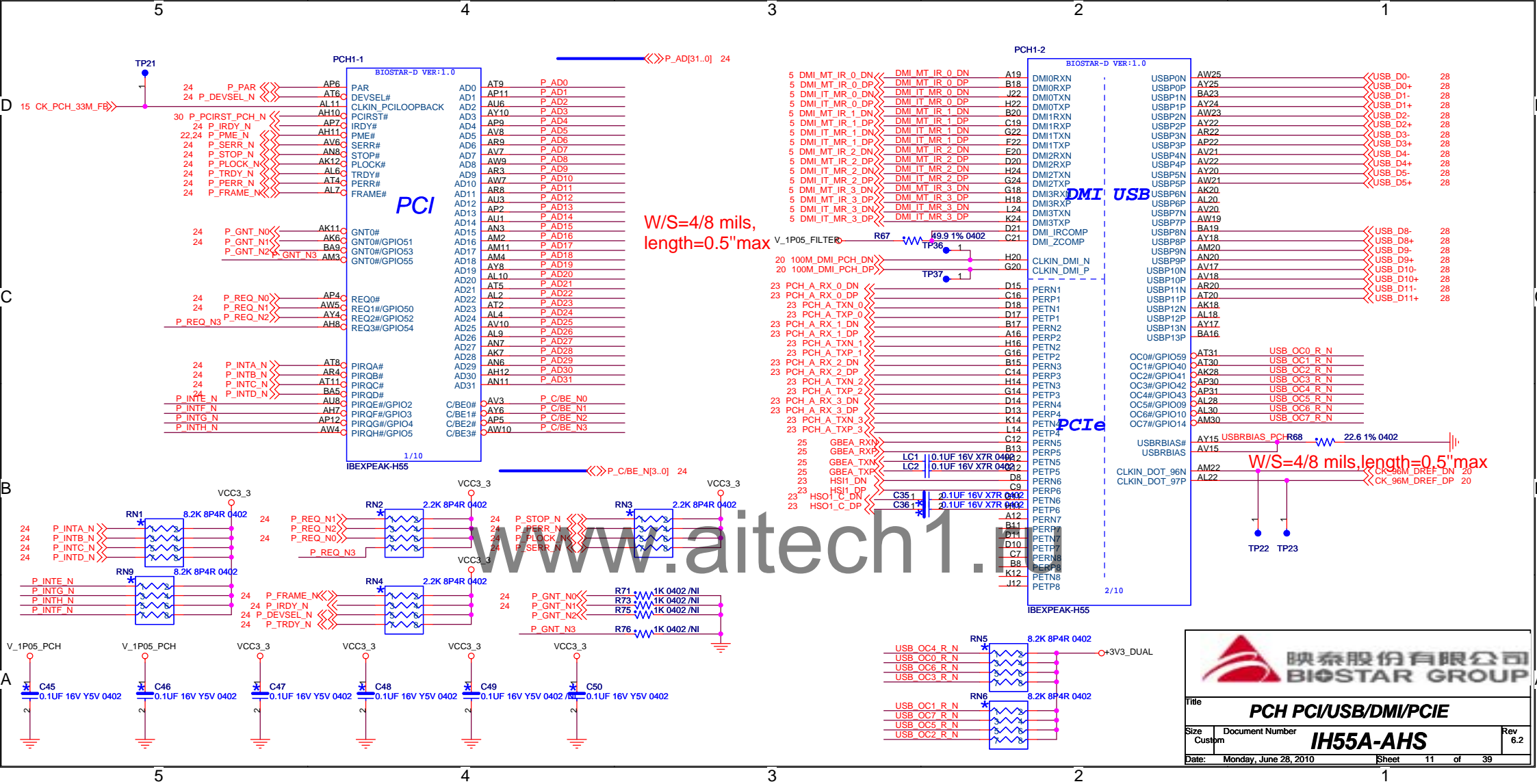
SA_DIMM_VREFDQ AG3 DIMM_DQ_OPT3_VREF_A
SB_DIMM_VREFDQ AG3 DIMM_DQ_OPT3_VREF_B

>>>DIMM_DQ_VREF_A 9
>>>DIMM_DQ_VREF_B 10

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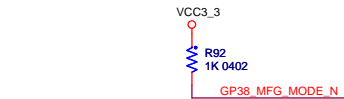
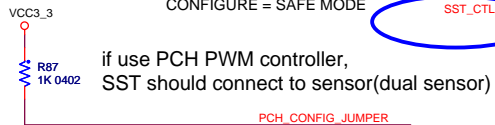


FOR SOP ENABLE AND FLASH
STUFF FOR RECOVERY USAGE ONLY

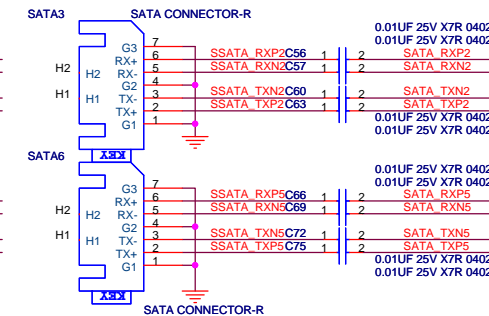
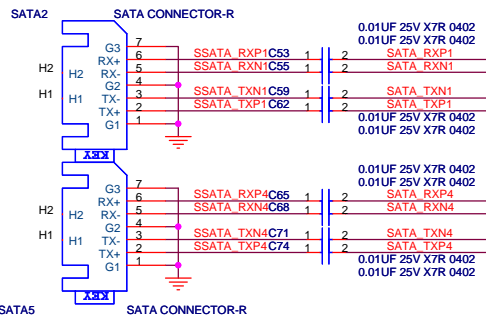
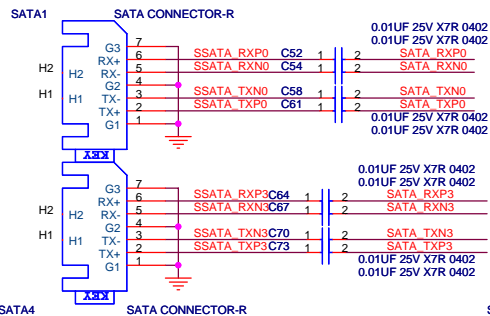
CONFIG / RECOVERY JUMPER

RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2	NORMAL (DEFAULT)
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY

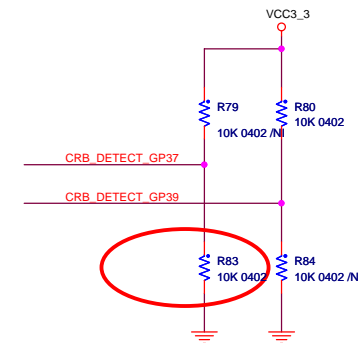
CONFIGURE = SAFE MODE



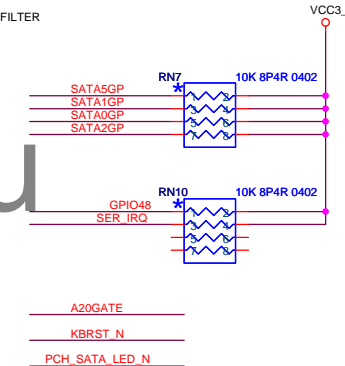
CONFIGURE = SAFE MODE



BOARDID TABLE: CRB STYLE

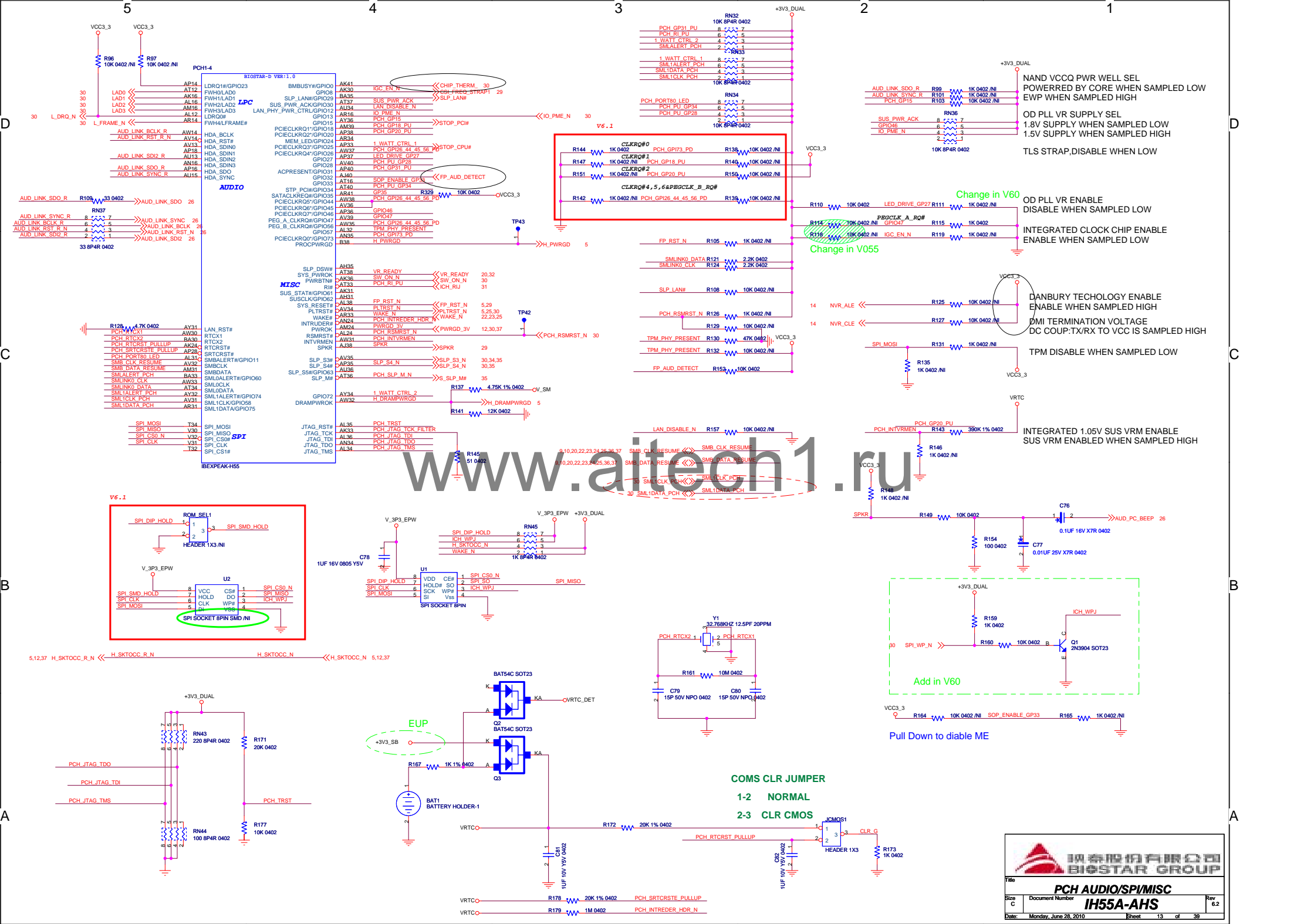


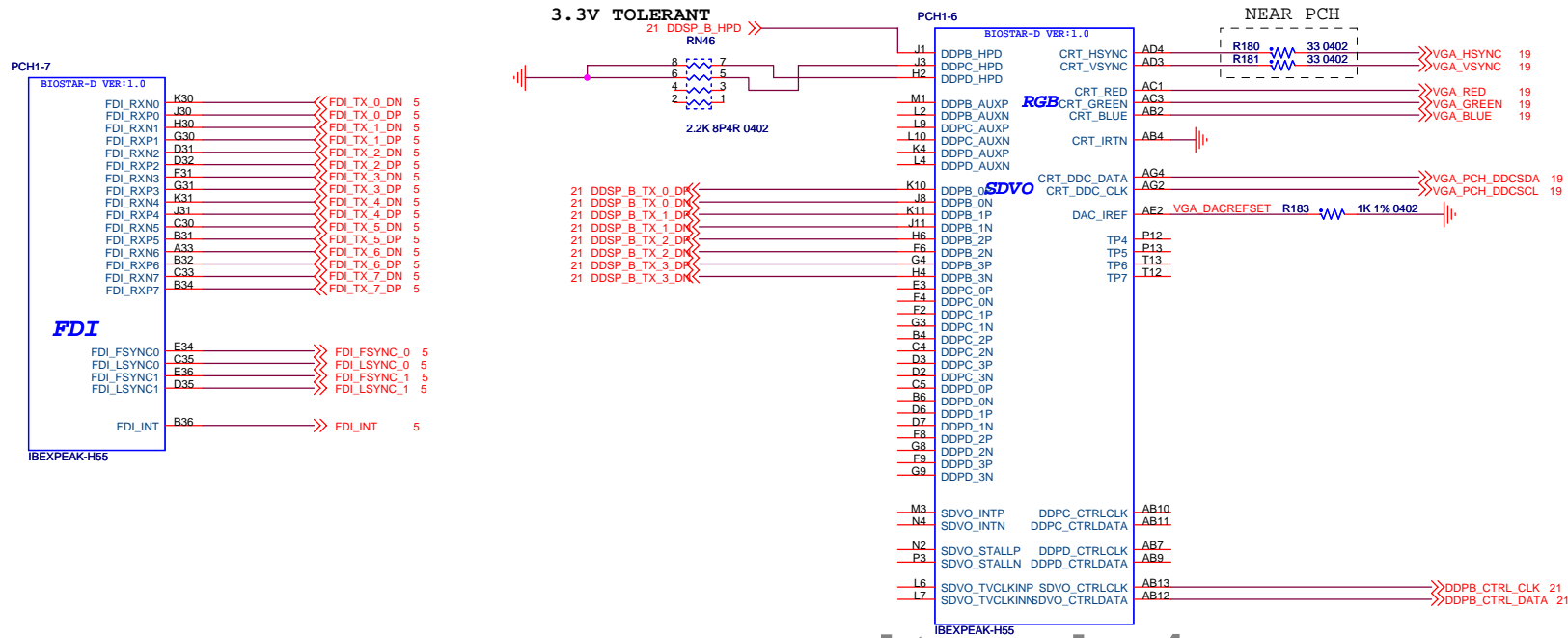
W/S=4/8 mils,length=0.5''max



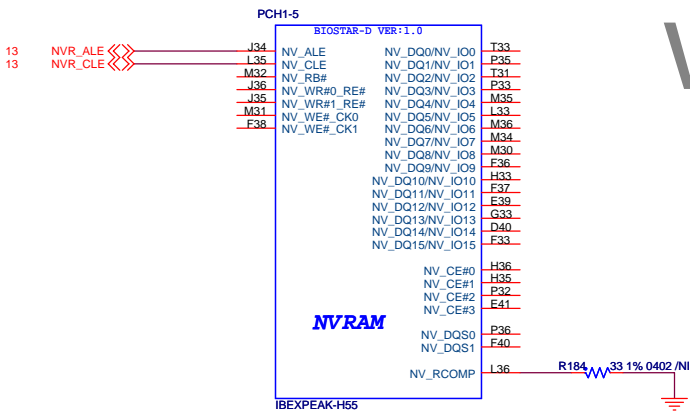
CONFIGURABLE CPU OUTPUT STRONGER IF LOW

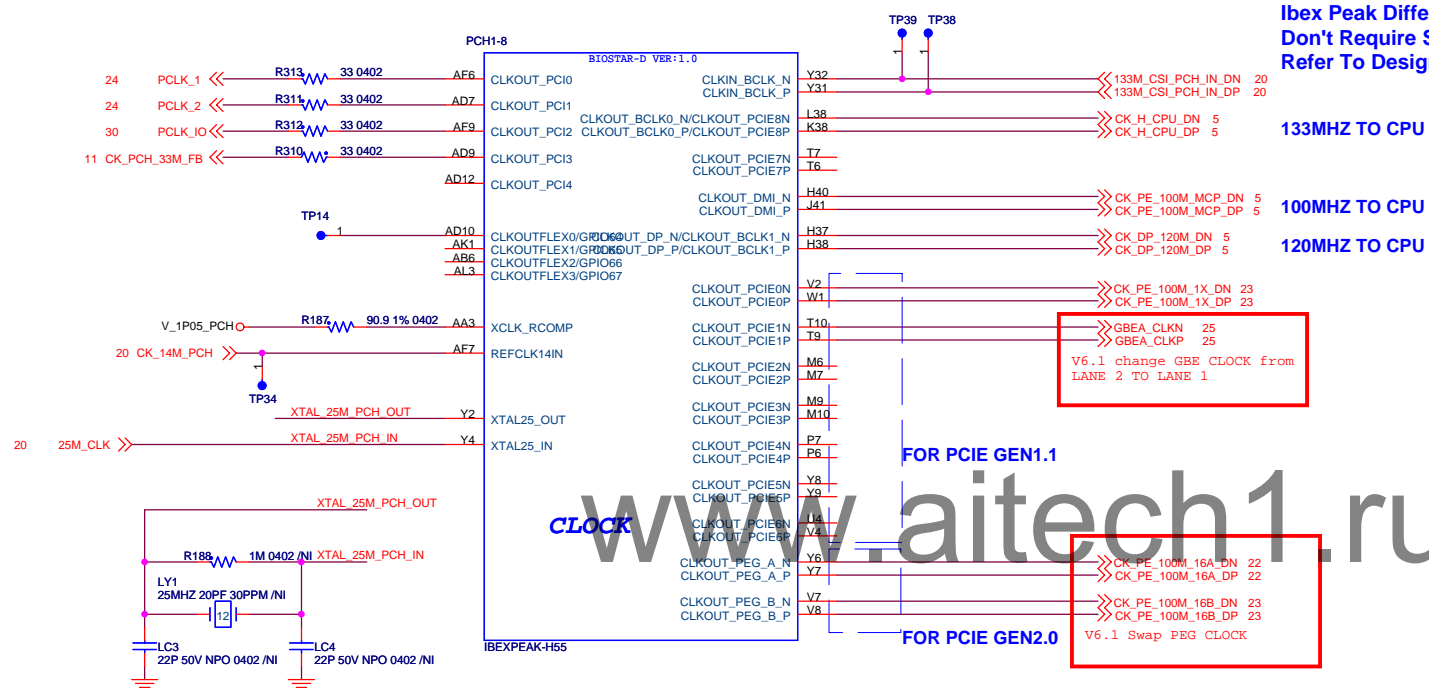
Title PCH SATA/CPU HOST		
Size	Document Number	Rev
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IBEX Peak Differential CLK Output
Don't Require Series Resistor
Refer To Design Guide P.106 /431.

133MHZ TO CPU

100MHZ TO CPU

120MHZ TO CPU

V6.1 change GBE CLOCK from
LANE 2 TO LANE 1

FOR PCIE GEN1.1

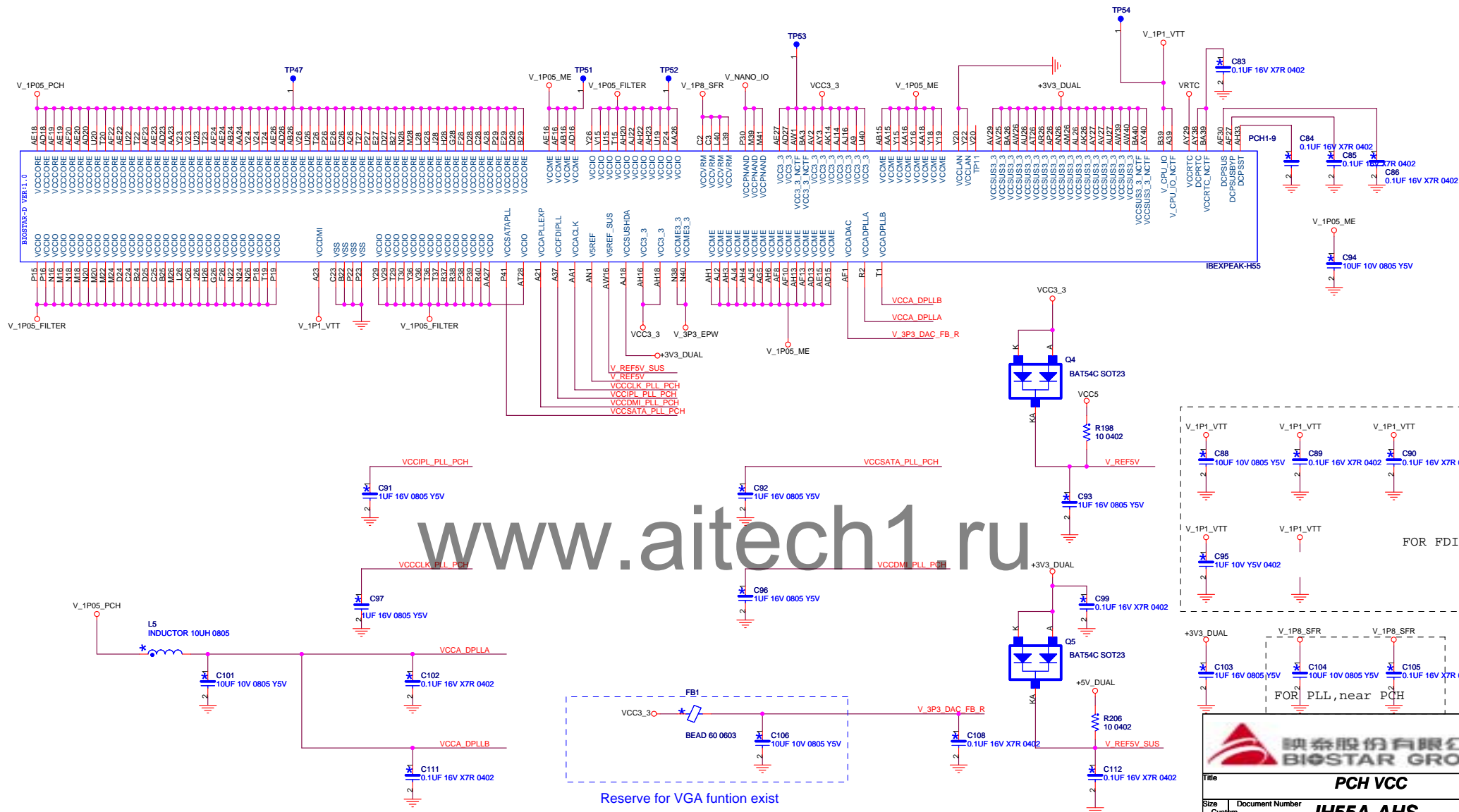
FOR PCIE GEN2.0

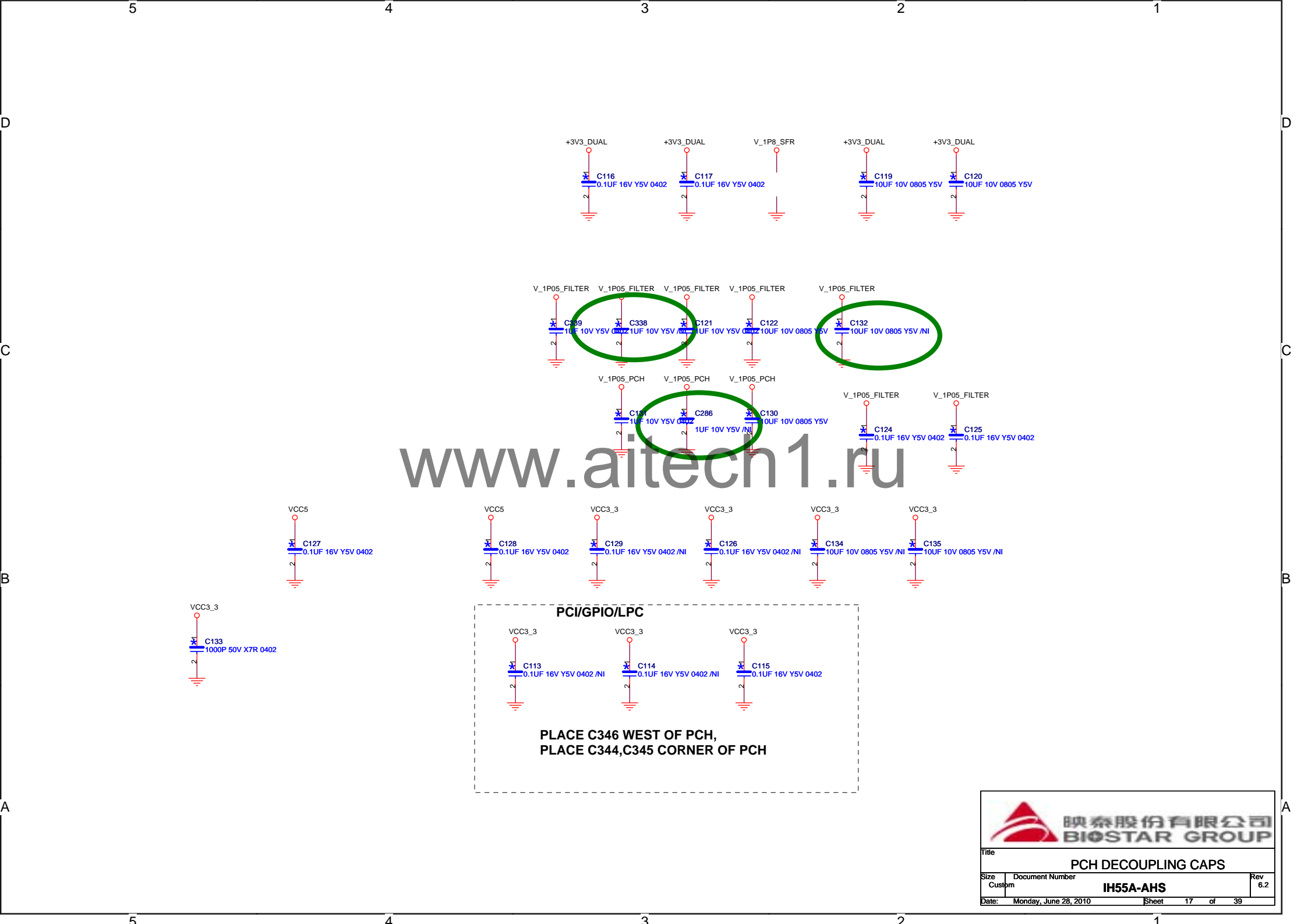
V6.1 Swap PEG CLOCK

$$C_e = 2 * C_L - (C_s + C_i)$$

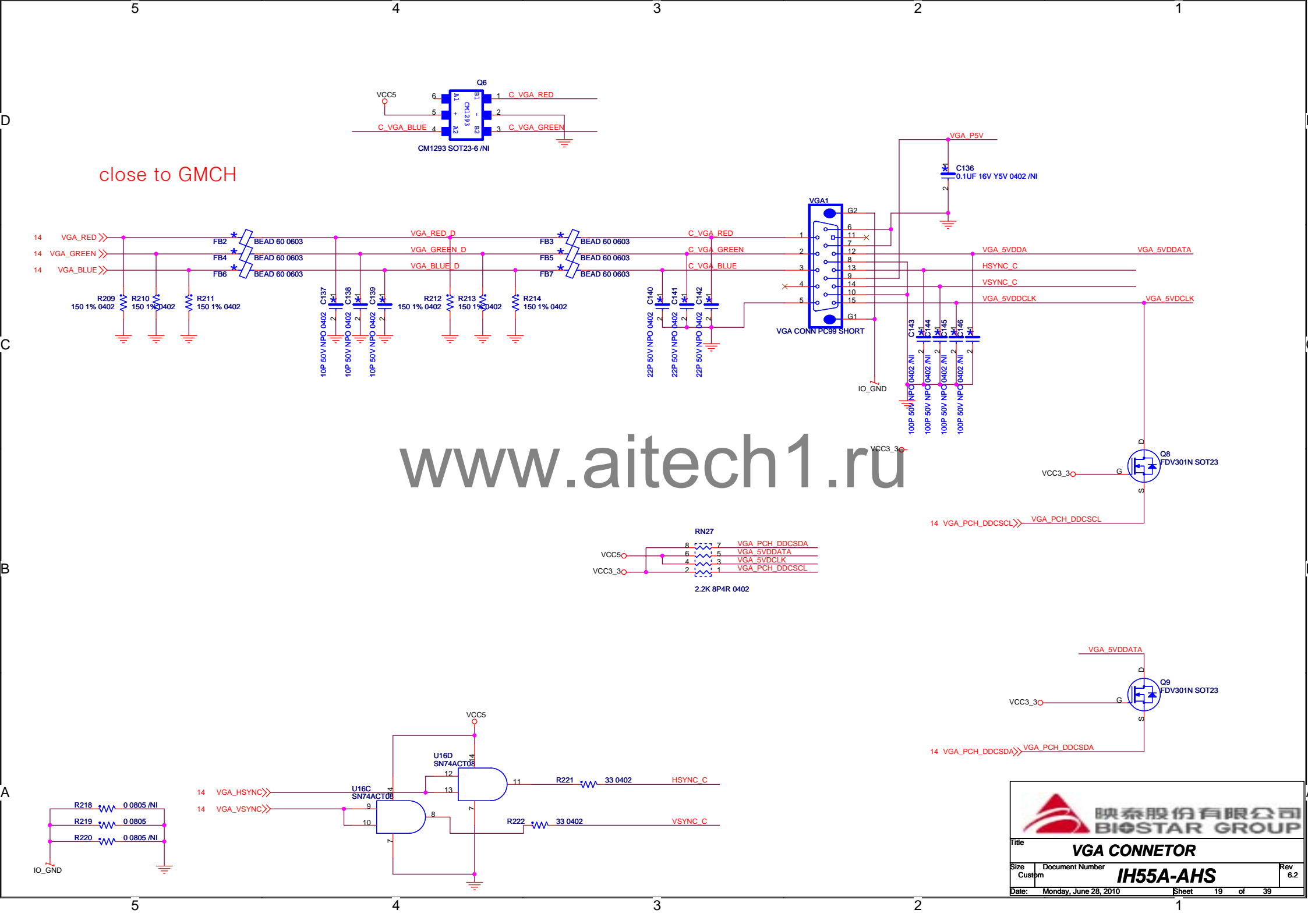
Ci: PIN CAPACITANCE IS 3-6 pF

Cs: trace capacitance is 3 to 10

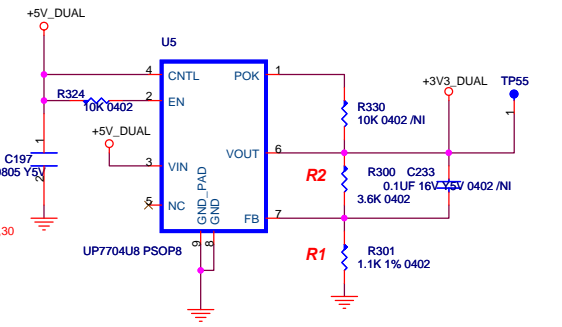
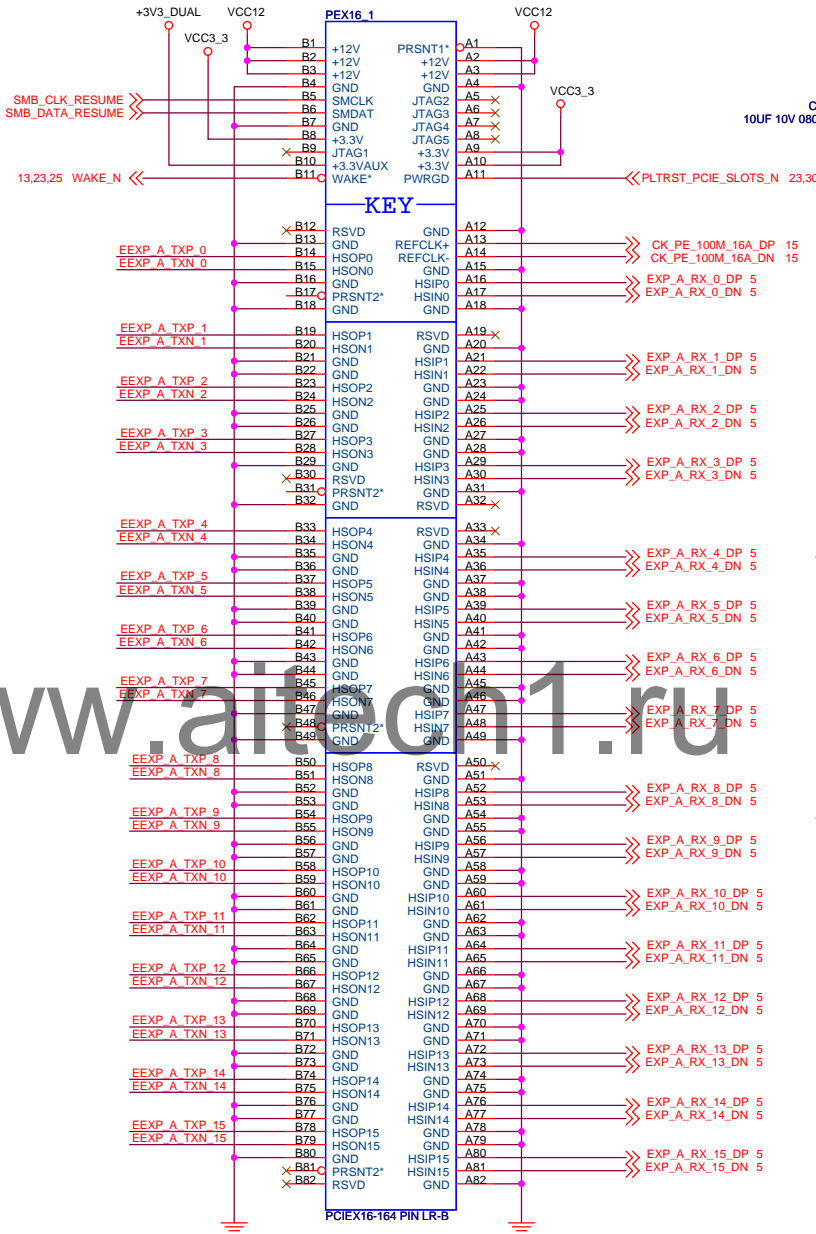






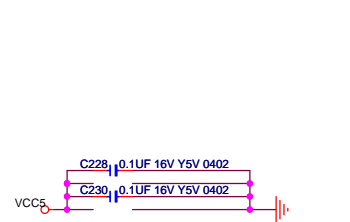
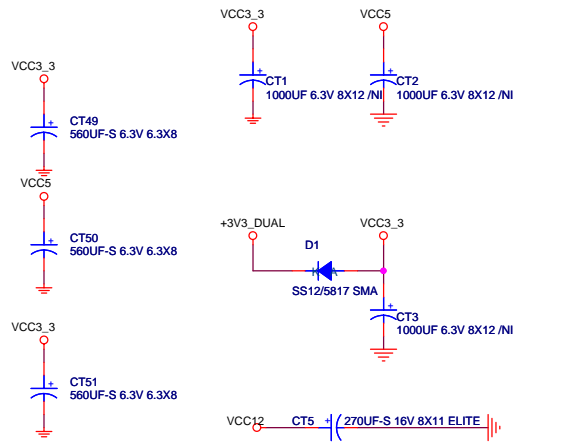
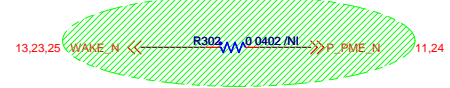


5	EXP_A_TX_0_DP	EXP_A_TXN_0	C198	1	2	0.1UF 16V X7R 0402	EEXP_A_TXP_0
5	EXP_A_TX_0_DN	EXP_A_TXN_0	C199	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_0
5	EXP_A_TX_1_DP	EXP_A_TXN_1	C200	1	2	0.1UF 16V X7R 0402	EEXP_A_TXP_1
5	EXP_A_TX_1_DN	EXP_A_TXN_1	C201	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_1
5	EXP_A_TX_2_DP	EXP_A_TXN_2	C202	1	2	0.1UF 16V X7R 0402	EEXP_A_TXP_2
5	EXP_A_TX_2_DN	EXP_A_TXN_2	C203	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_2
5	EXP_A_TX_3_DP	EXP_A_TXN_3	C204	1	2	0.1UF 16V X7R 0402	EEXP_A_TXP_3
5	EXP_A_TX_3_DN	EXP_A_TXN_3	C205	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_3
5	EXP_A_TX_4_DP	EXP_A_TXN_4	C206	1	2	0.1UF 16V X7R 0402	EEXP_A_TXP_4
5	EXP_A_TX_4_DN	EXP_A_TXN_4	C207	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_4
5	EXP_A_TX_5_DP	EXP_A_TXN_5	C208	1	2	0.1UF 16V X7R 0402	EEXP_A_TXP_5
5	EXP_A_TX_5_DN	EXP_A_TXN_5	C209	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_5
5	EXP_A_TX_6_DP	EXP_A_TXN_6	C210	1	2	0.1UF 16V X7R 0402	EEXP_A_TXP_6
5	EXP_A_TX_6_DN	EXP_A_TXN_6	C211	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_6
5	EXP_A_TX_7_DP	EXP_A_TXN_7	C212	1	2	0.1UF 16V X7R 0402	EEXP_A_TXP_7
5	EXP_A_TX_7_DN	EXP_A_TXN_7	C213	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_7
5	EXP_A_TX_8_DP		C214	1	2	0.1UF 16V X7R 0402	EEXP_A_TXP_8
5	EXP_A_TX_8_DN		C215	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_8
5	EXP_A_TX_9_DP		C216	1	2	0.1UF 16V X7R 0402	EEXP_A_TXP_9
5	EXP_A_TX_9_DN		C217	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_9
5	EXP_A_TX_10_DP		C218	1	2	0.1UF 16V X7R 0402	EEXP_A_TXP_10
5	EXP_A_TX_10_DN		C219	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_10
5	EXP_A_TX_11_DP		C220	1	2	0.1UF 16V X7R 0402	EEXP_A_TXP_11
5	EXP_A_TX_11_DN		C221	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_11
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5	EXP_A_TX_13_DP		C224	1	2	0.1UF 16V X7R 0402	EEXP_A_TXP_13
5	EXP_A_TX_13_DN		C225	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_13
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5	EXP_A_TX_14_DN		C227	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_14
5	EXP_A_TX_15_DP		C229	1	2	0.1UF 16V X7R 0402	EEXP_A_TXP_15
5	EXP_A_TX_15_DN		C231	1	2	0.1UF 16V X7R 0402	EEXP_A_TXN_15



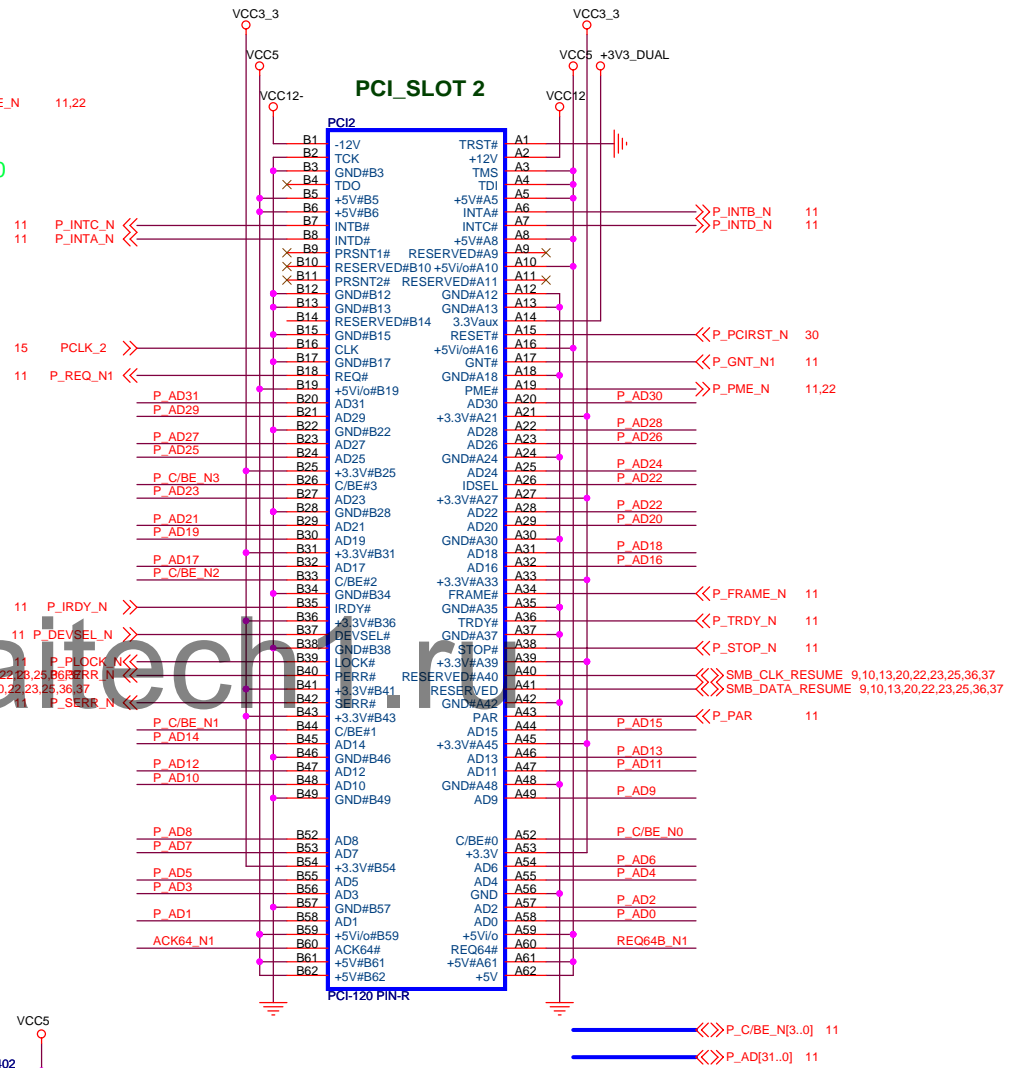
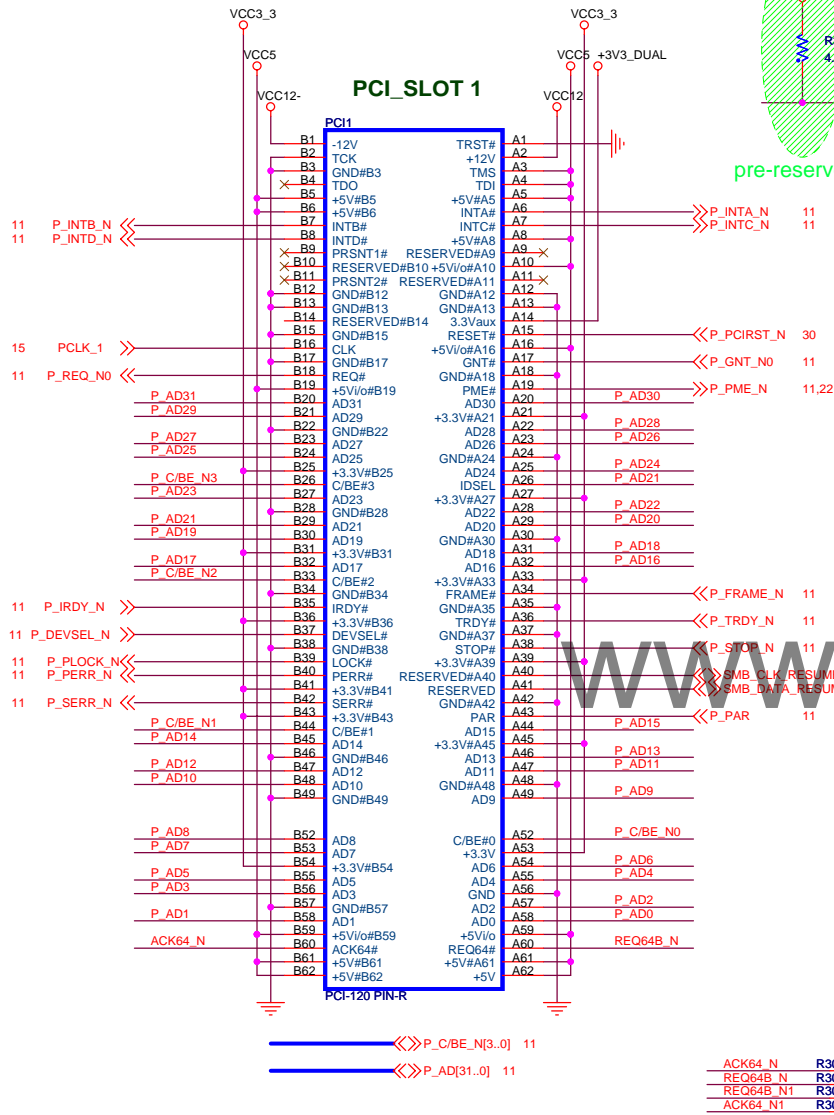
$$V_{out} = V_{ref} (0.8V) \times (R2/R1 + 1) = 3.42V$$

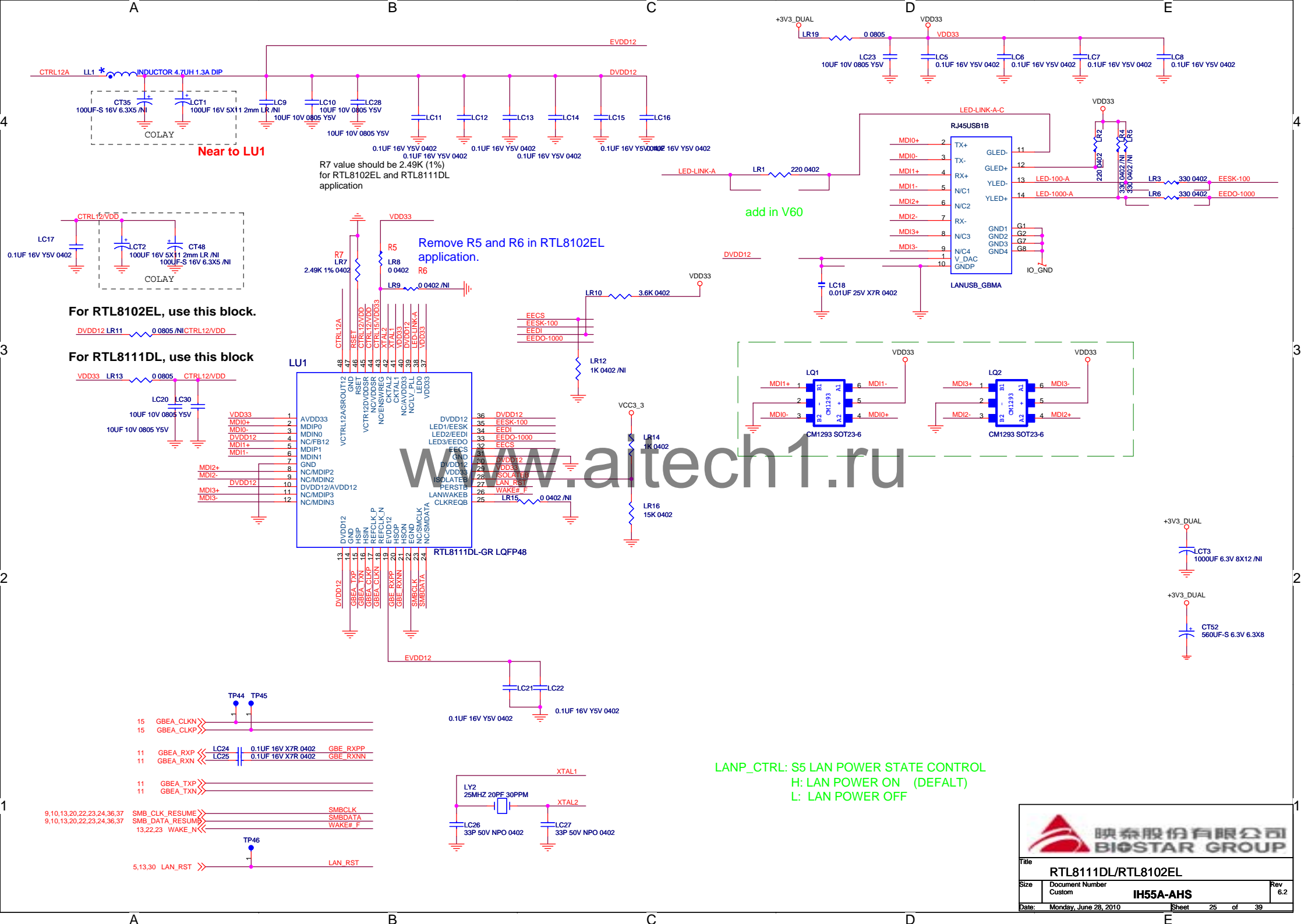
Pre-reserve in V60

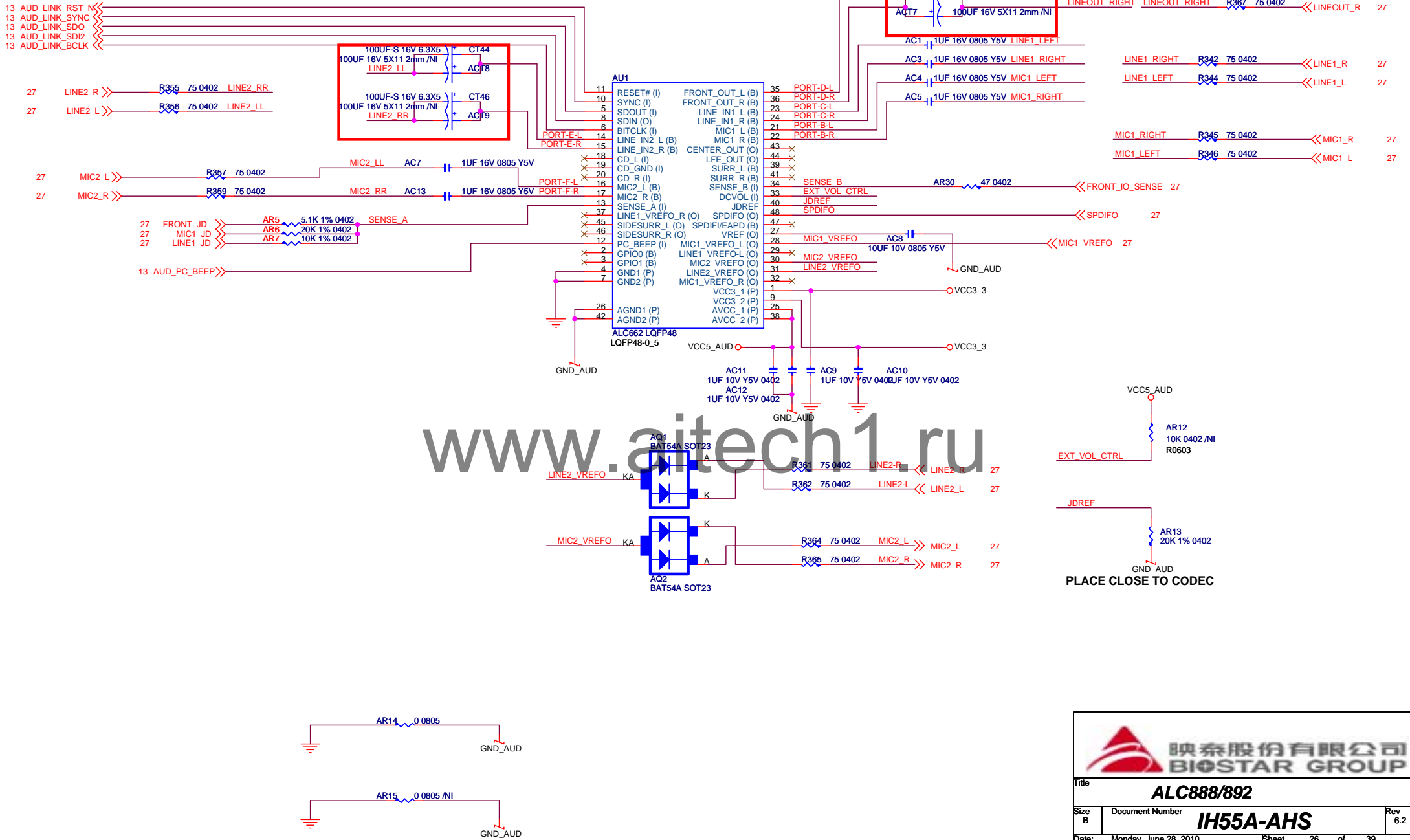


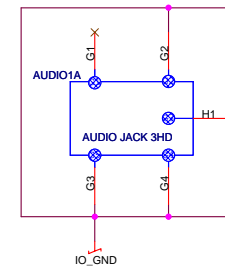
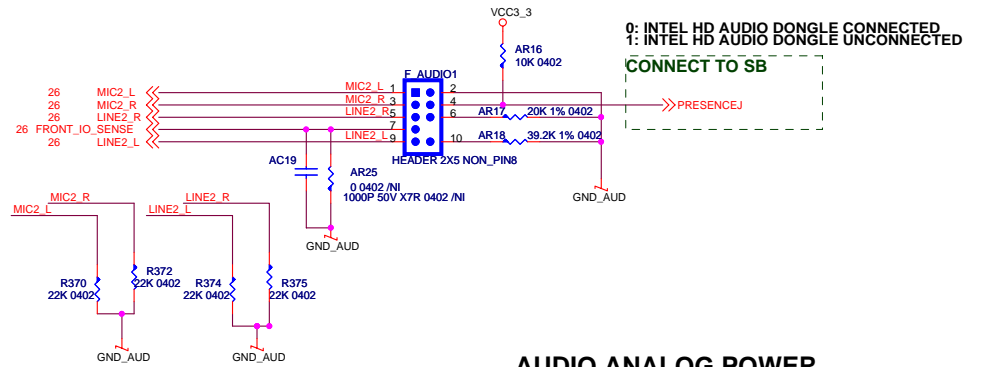
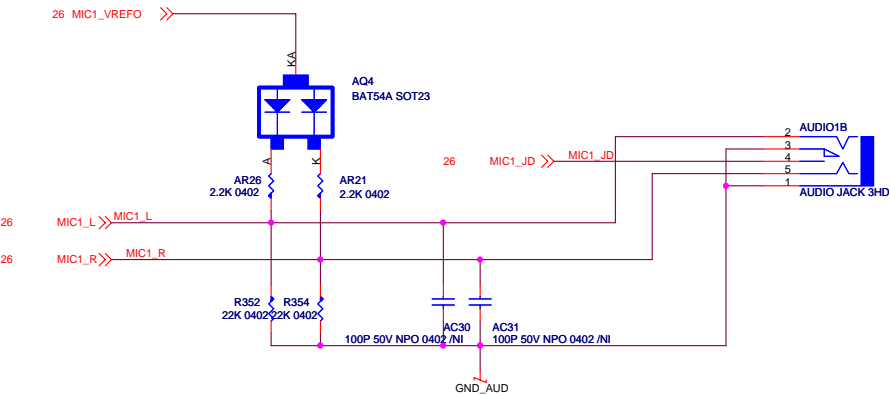
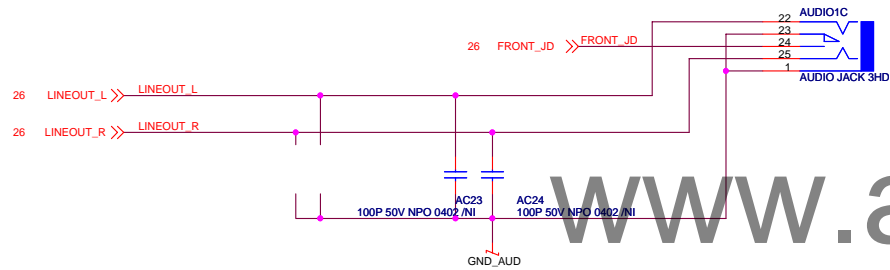
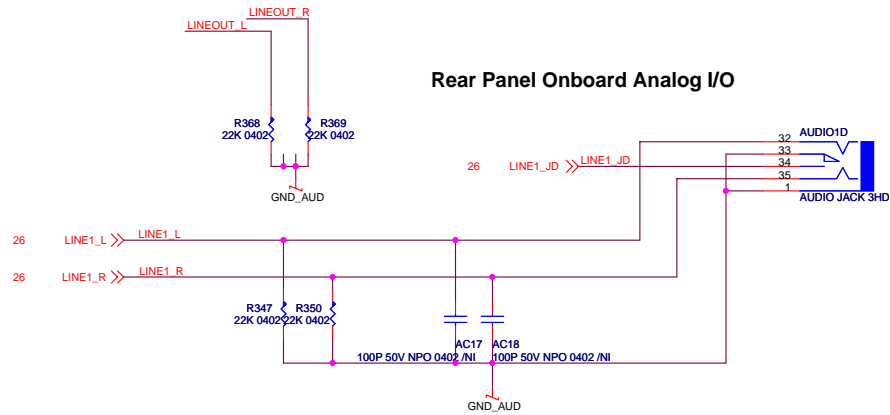
IDSEL:AD21, INT:ABCD, REQ0 & GNT0, PCI_CLK1

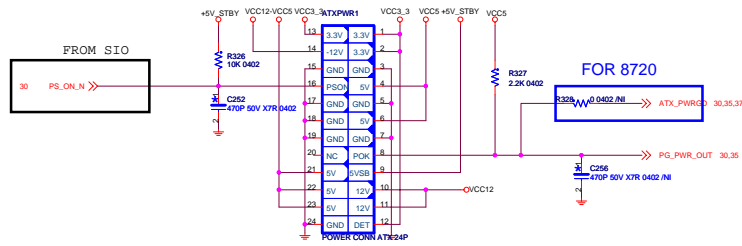
IDSEL:AD22, INT:BCDA, REQ1 & GNT1, PCI_CLK2





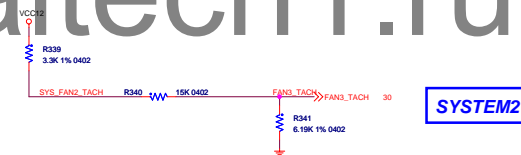
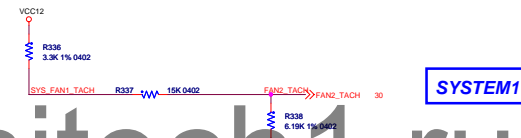
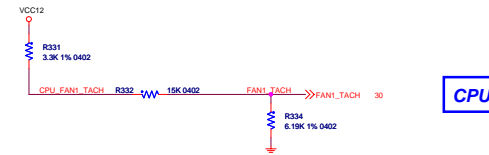
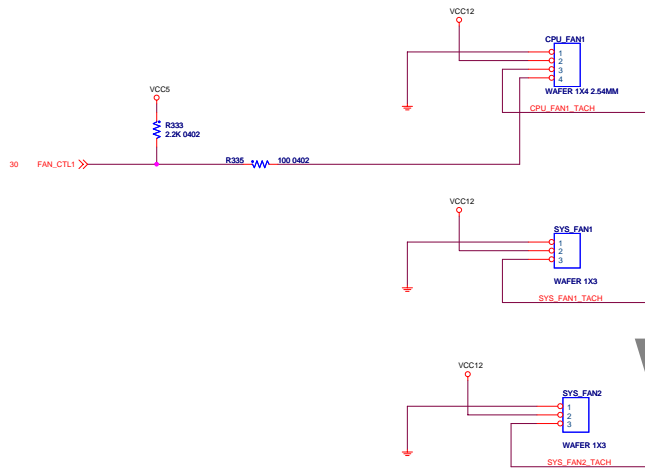




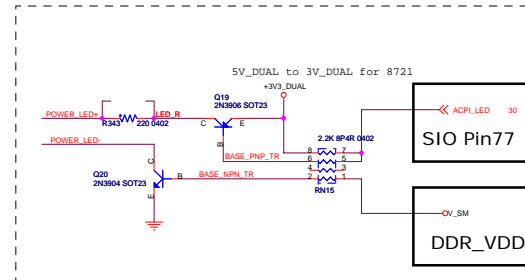
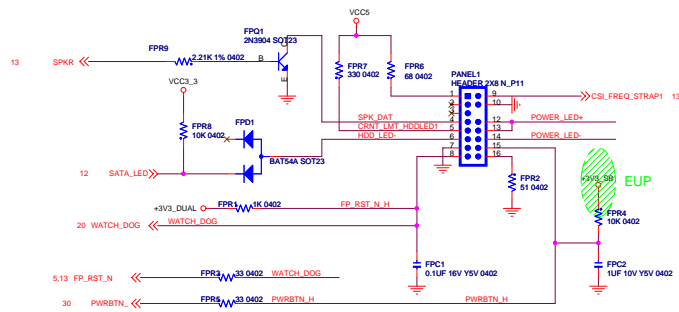


EMI POWER CONN DECOUPLING

CPU FAN/SYSTEM FAN1/SYSTEM FAN2



FRONT PANEL HEADER



LED_D2	LED_D1	MESSAGE
OFF	OFF	ABNORMAL
OFF	ON	MEMORY ERROR
ON	OFF	VGA ERROR
ON	ON	NORMAL

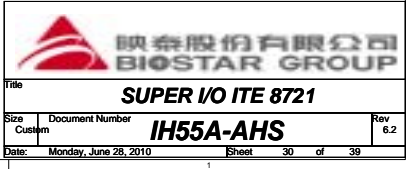
FOR T-SERIAL



Title	FAN&POWER CONN&FP
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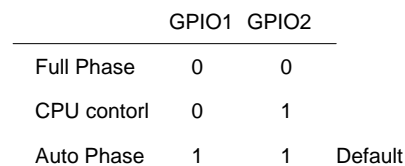
Size	Document Number	IH55A-AHS
Custom		

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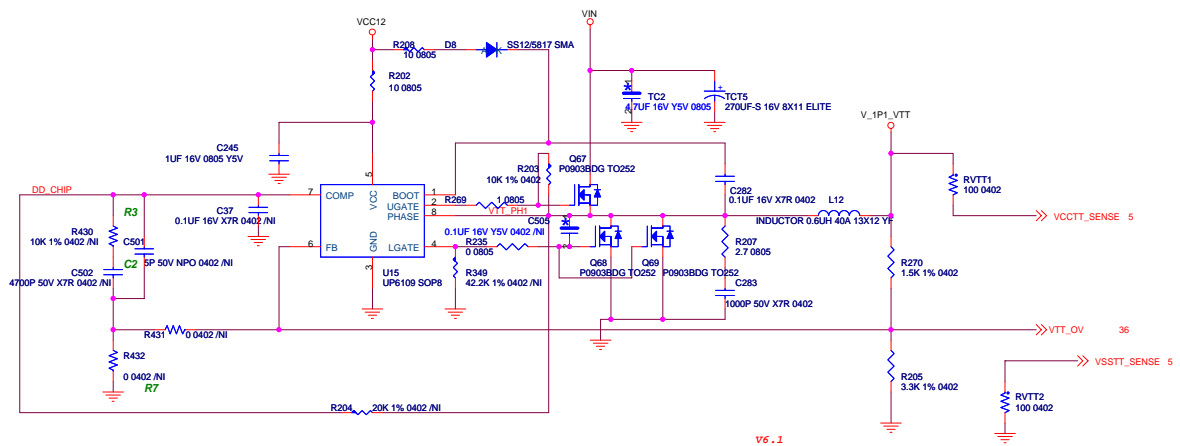




Title			
FDD / PS2 CONN			
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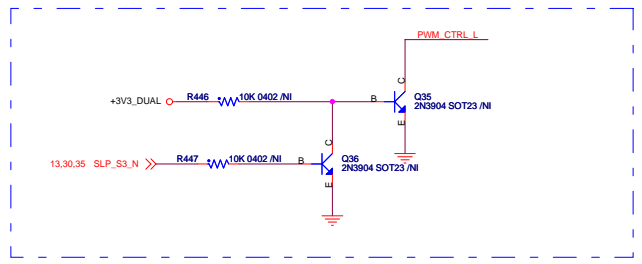
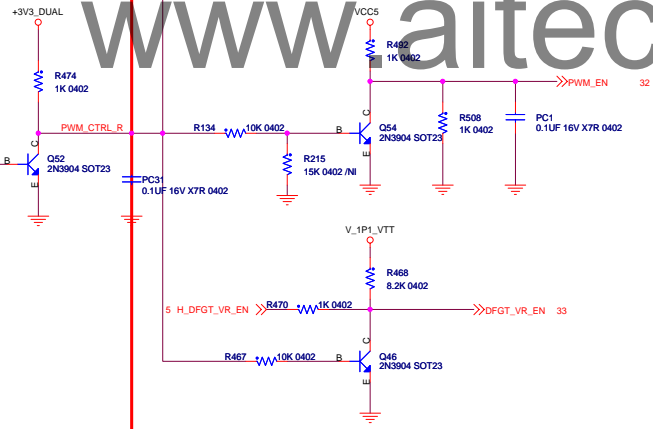
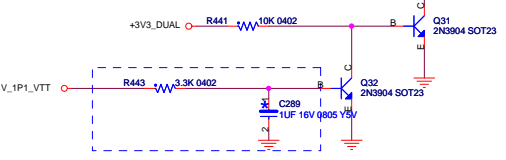




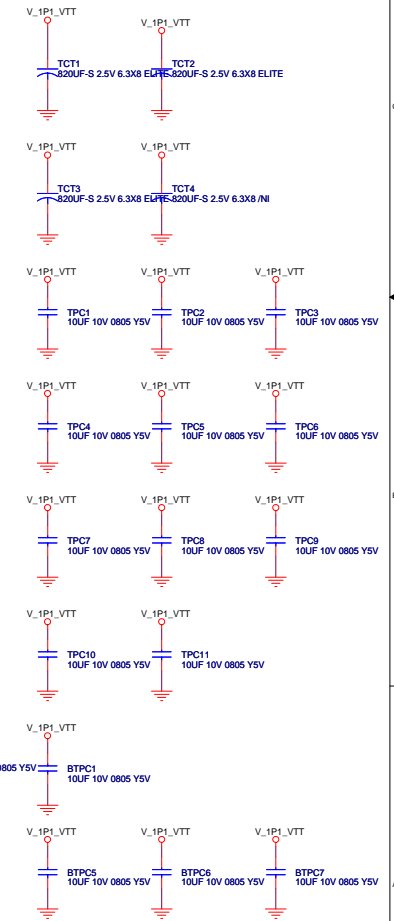


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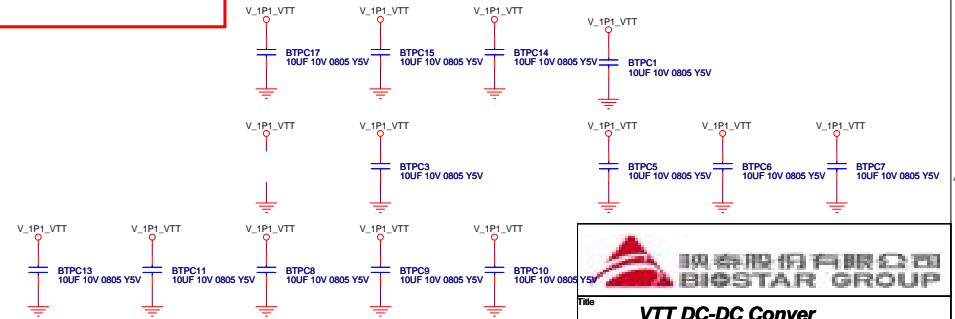
For delay 100ns min, 50ms max

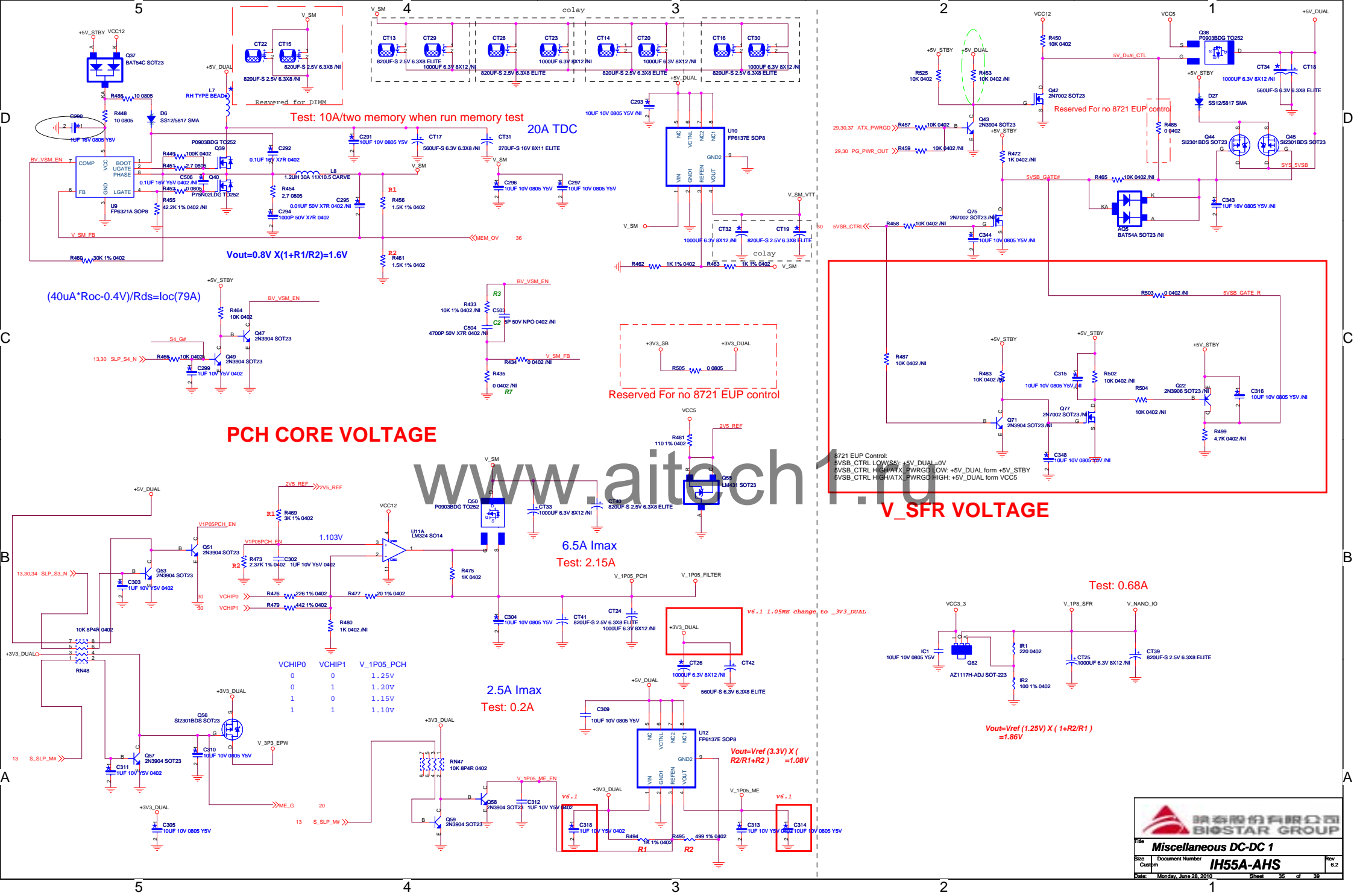


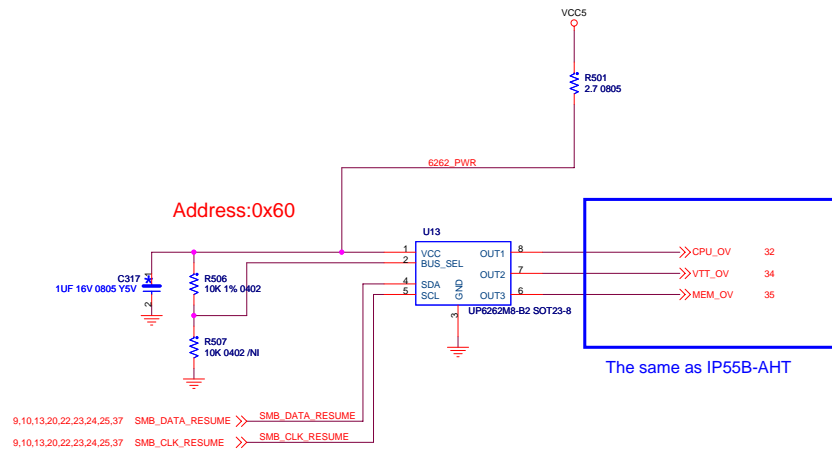
1.1V/48A



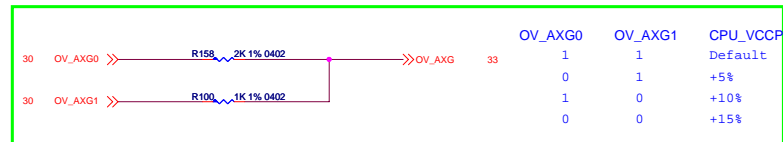
TBD





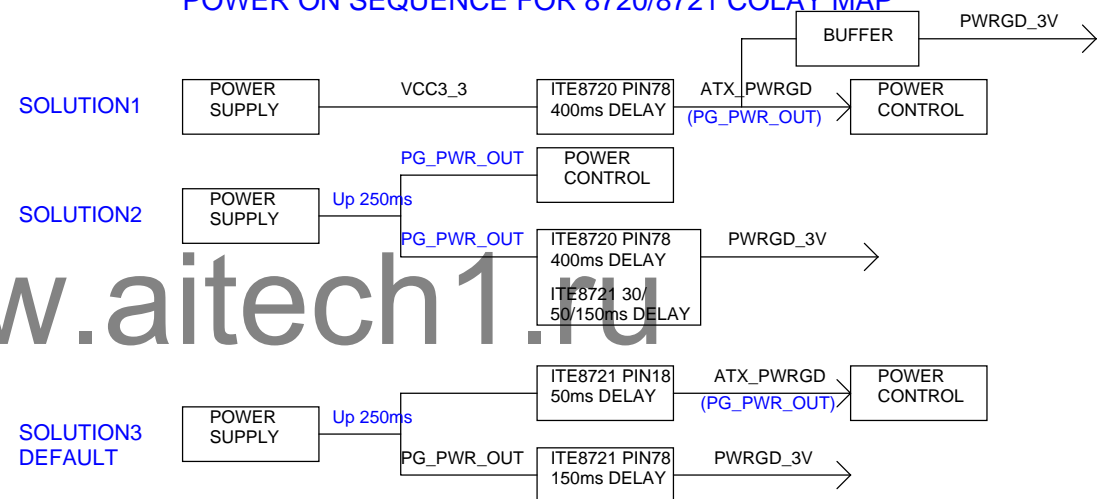


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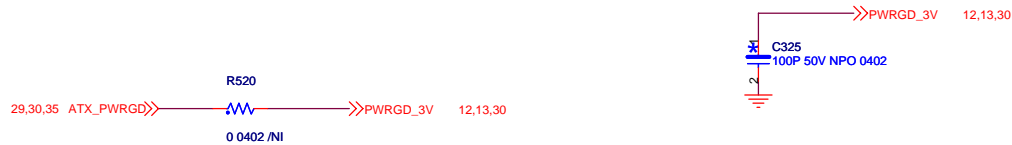




POWER ON SEQUENCE FOR 8720/8721 COLAY MAP



FALL TIME:40mv/us



PWM Frequency Control--V6.0 DISABLE

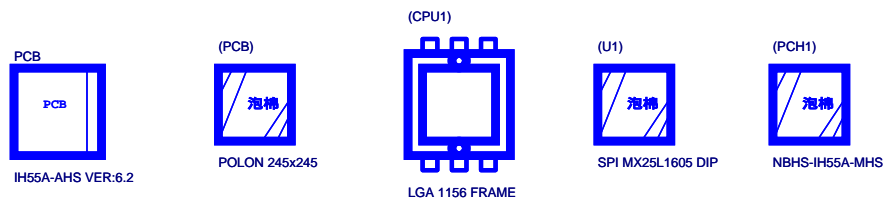
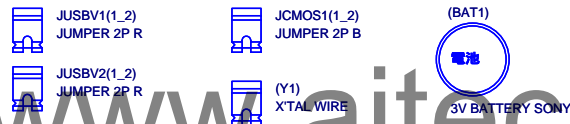
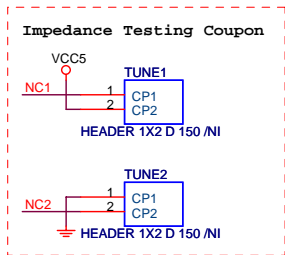
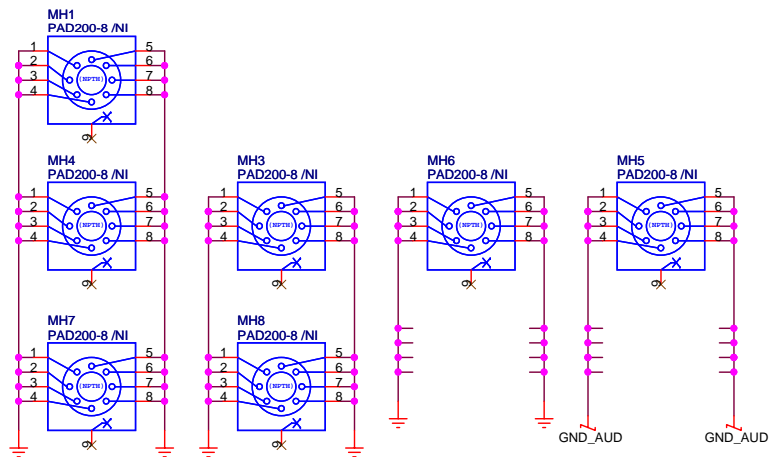
6206:Fsw=1000/Rosc(Kohm)
=200kHz
6219:Fsw=300*(24K/Rosc)^{0.92}
=200kHz

PWM_CTL1	PWM_CTL2	FREQUENCY
0	0	220K
0	1	180K
1	0	240K
1	1	200K

default

Fixed INTEL 1156 SOCKET coolbug ISSUE

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